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Search History

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L11	L9 same (device or chip or ic)	33	L11
L10	L8 same (device or chip or ic)	23	L10
L9	L6 same voltage	80	L9
L8	L6 same current	65	L8
L7	L6 same adjust$	6	L7
L6	L1 same circuit same measur$	116	L6
L5	L3 same l1	9	L5
L4	l1 and l1	6429	L4
L3	self-test$	8991	L3
L2	L1 same measur$ same $test$	24	L2
L1	internal near2 power near2 supply	6429	L1

END OF SEARCH HISTORY

L2: Entry 11 of 24 File: USPT Apr 7, 1998

DOCUMENT-IDENTIFIER: US 5736894 A
TITLE: Semiconductor device and method of adjusting internal power supply potential of the semiconductor device

Detailed Description Text (14):
First, test mode signal .phi.1 is set to the "L" level, test mode signal .phi..sub.2 is set to the "H" level so that V.sub.2 =0V, and internal power supply potential intVcc is measured at a point where extVcc=Va. At this time, since V.sub.2 =0V, it holds that intVcc=V.sub.1. Thereafter, difference voltage .DELTA.a between the set value of V.sub.1 and the measured value of intVcc=V.sub.1 at the point where extVcc=Va is calculated, and resistance values R.sub.3 and R.sub.1 of variable resistance circuits 8 and 15 are adjusted, whereby V.sub.1 is raised by difference voltage .DELTA.a. Consequently, the curve V.sub.N1 of FIG. 2 can be corrected to the line of V.sub.N1 '.

Detailed Description Text (15):
Thereafter, test mode signal .phi..sub.1 is set to "H" level, test mode signal .phi..sub.2 is set to the "L" level so that V.sub.1 =0V, and internal power supply potential intVcc where extVcc=Vb is measured. At this time, since V.sub.1 =0V, it holds that intVcc=V.sub.2. Thereafter, difference voltage .DELTA.b between the measured value of intVcc=V.sub.2 and the set value of V.sub.2 at the point where extVcc=Vb is calculated, resistance values R.sub.4 and R.sub.2 of variable resistance circuits 19 and 22 are adjusted and thus V.sub.2 is lowered by the difference voltage .DELTA.b. Thus the line V.sub.N2 of FIG. 3 can be corrected to the curve V.sub.N2 '.

Detailed Description Text (29):
First, in the similar manner as in Embodiment 1, the difference voltage .DELTA.a between the set value of V.sub.1 and the measured value at the point where extVcc=Va is calculated. Thereafter, test mode signal .phi..sub.3 is set to the "H" level so that P channel MOS transistor 37 is rendered non-conductive. Consequently, series resistance value of variable resistance circuit 8 and test circuit 26 increases from R.sub.3 to R.sub.3 +.phi.R.sub.3, current value I.sub.1 reduces and V.sub.1 lowers. The characteristic part of internal power supply potential intVcc at this time corresponds to V.sub.N11 of FIG. 5. The internal power supply potential intVcc=V.sub.1 at the point where extVcc=Va is measured, and the difference voltage .DELTA.a.sub.1 of V.sub.1 before and after the test mode signal .phi..sub.3 is set to "H" level is calculated. More specifically, the change .DELTA.a.sub.1 of V.sub.1 with respect to the change .DELTA.R.sub.3 of the resistance value of constant current circuit 32 is actually measured.

Detailed Description Text (30):
Thereafter, test mode signal .phi..sub.3 is recovered to the "L" level, and test mode signal .phi..sub.4 is set to "L" level. Consequently, series resistance value of variable resistance circuit 15 and test circuit 27 increases from R.sub.1 to R.sub.1 +.DELTA.R.sub.1, and V.sub.1 rises. The characteristic curve of internal power supply potential intVcc at this time corresponds to V.sub.N12 of FIG. 5. At this state, internal power potential intVcc =V.sub.1 is measured at a point where extVcc=Va, and difference voltage .DELTA.a.sub.2 before and after the test mode signal .phi..sub.4 is set to the "H" level is calculated. In other words, the

change .DELTA.a.sub.2 of V.sub.1 with respect to the change .DELTA.R.sub.1 of the resistance value of V.sub.2 generating circuit 33 is actually measured. It is possible to correct the deviation of V.sub.1 from the set value, based on the two values .DELTA.a.sub.1 and .DELTA.a.sub.2. FIG. 5 shows an example in which the measured value is lower than the set value of V.sub.1. In that case, by increasing resistance value R.sub.1 of V.sub.1 generating circuit 33, V.sub.1 can be corrected. The necessary value of correction of the resistance in this case is represented as (.DELTA.a/.DELTA.a.sub.2).times..DELTA.R.sub.1. Conversely, if the measured value of V.sub.1 is higher than the set value, resistance value R.sub.3 of constant current circuit 32 is increased and current I.sub.1 is reduced so that V.sub.1 is lowered to be equal to the set value. The necessary value of correction of the resistance in this case is represented as (.DELTA.a/.DELTA.a.sub.1).times..DELTA.R.sub.3.

Detailed Description Text (31):
The method of adjusting V.sub.2 will be described. First, in the similar manner as Embodiment 1, difference voltage .DELTA.b between the set value and the measured value of V.sub.2 at the point where ExtVcc =Va is calculated. Thereafter, test mode signal .phi..sub.6 is set to the "H" level so that P channel MOS transistor 43 is rendered non-conductive. Consequently, series resistance value of variable resistance circuit 22 and test circuit 29 increases from R.sub.2 to R.sub.2 +.DELTA.R.sub.2, and V.sub.2 lowers from extVcc-I.sub.2 .times.R.sub.2 to extVcc-(R.sub.2 +.DELTA.R.sub.2). Characteristic curve of the internal power supply potential IntVcc at this time corresponds to V.sub.N21 of FIG. 6. At this state, the internal power supply potential intVcc=V.sub.2 at the point where extVcc=Vb is measured, and difference voltage .DELTA.b1 of V.sub.2 before and after the test mode signal .phi..sub.6 is set to the "H" level is calculated. In other words, the change .DELTA.b.sub.1 of V.sub.2 with respect to the change .DELTA.R.sub.2 of the resistance value of V.sub.2 generating circuit 35 is actually measured.

Detailed Description Text (32):
Thereafter, test mode signal .phi..sub.6 is returned to the "L" level, and test mode signal .phi..sub.5 is set to the "H" level. Consequently, series resistance value of variable resistance circuit 19 and test circuit 28 increases form R.sub.4 to R.sub.4 +.DELTA.R.sub.4, current value of I.sub.2 reduces and V.sub.2 increases. The characteristic curve of internal power supply potential intVcc at this time corresponds to V.sub.N22. At this state, internal power supply potential intVcc=V.sub.2 at the point where extVcc=Vb is measured, and difference voltage .DELTA.b.sub.2 before and after the test mode signal .phi..sub.5 is set to the "H" level is calculated. In other words, the change .DELTA.b.sub.2 of V.sub.2 with respect to the change .DELTA.R.sub.4 of the resistance value of the constant current circuit 34 is actually measured.

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US005736894A

United States Patent [19]

Suwa

[11] Patent Number: 5,736,894

[45] Date of Patent: Apr. 7, 1998

[54] **SEMICONDUCTOR DEVICE AND METHOD OF ADJUSTING INTERNAL POWER SUPPLY POTENTIAL OF THE SEMICONDUCTOR DEVICE**

[75] Inventor: **Makoto Suwa**, Hyogo, Japan

[73] Assignee: **Mitsubishi Denki Kabushiki Kaisha**, Tokyo, Japan

[21] Appl. No.: **559,052**

[22] Filed: **Nov. 16, 1995**

[30] **Foreign Application Priority Data**

Apr. 26, 1995 [JP] Japan 7-102254

[51] **Int. Cl.**[6] **G05F 1/10**

[52] **U.S. Cl.** **327/538**; 327/530; 327/540

[58] **Field of Search** 327/530, 538, 327/540, 543, 535, 541; 365/189.09

[56] **References Cited**

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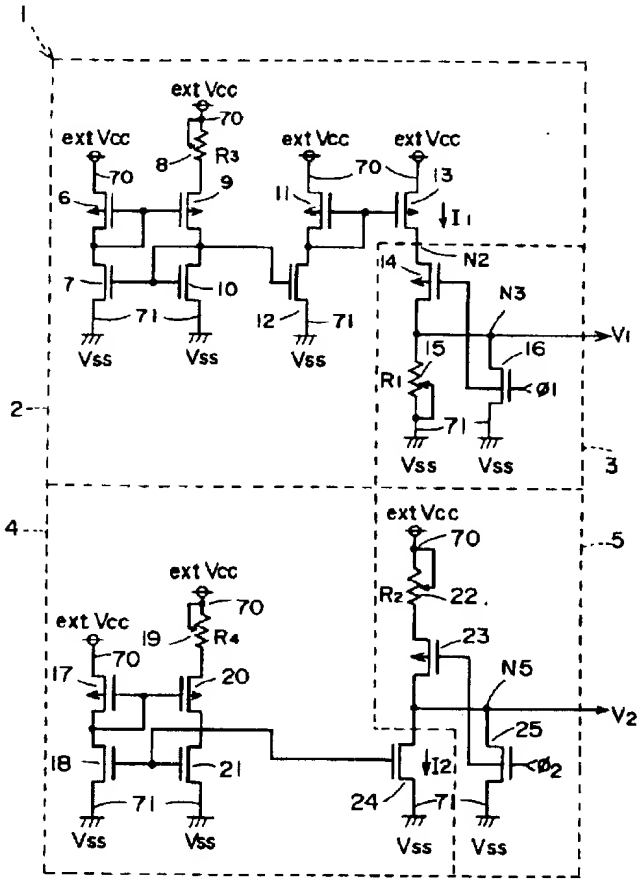
Primary Examiner—Timothy P. Callahan
Assistant Examiner—Jung Ho Kim
Attorney, Agent, or Firm—Lowe, Price, LeBlanc & Becker

[57] **ABSTRACT**

In a level generating circuit 1 included in an internal power supply circuit of a DRAM, MOS transistors **14** and **16** for inactivating a V_1 generating circuit **3**, and MOS transistors **23** and **25** for inactivating a V_2 generating circuit **5** are provided. When V_1 is to be adjusted, V_2 generating circuit **5** is inactivated, and when V_2 is to be adjusted, V_1 generating circuit **3** is inactivated. Therefore, failure of adjustment of internal power supply potential intVcc caused by confusion of V_1 and V_2 can be prevented.

10 Claims, 10 Drawing Sheets



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L5: Entry 1 of 9 File: USPT Mar 11, 2003

DOCUMENT-IDENTIFIER: US 6532183 B2
TITLE: Semiconductor device capable of adjusting internal potential

Detailed Description Text (3):
FIG. 1 is a block diagram showing the structure of a system LSI 1 according to a first embodiment of the present invention. Referring to FIG. 1, this system LSI 1 comprises a logic circuit part 2, a memory circuit part 3, an internal power supply potential generation circuit 4 and a BIST (built-in self-testing) circuit 5.

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